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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,231	12/04/2001	Alain Benayoun	FR920000052	8295

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EXAMINER	
QURESHI, AFSAR M	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,231	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Afsar M. Qureshi	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Amendments received on November 11/12/2004 are entered as requested.

2. In light of the amendments to Specification, drawings and claims, all objections as in the previous Office action, dated 8/12/2004, are removed. Also, rejection of claim 4, under 35 USC § 112, 2nd paragraph is withdrawn.

3. ***The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.***

4. Claims 1, 8, 9, and 10 is rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Pat. No. 6,501,734 issued to Yu et al (hereinafter Yu).

Regarding claims 1, 8, 9, and 10 Yu discloses a switching module , a switching structure, a cross-connected switching structure and a switch in a data transmission system comprising:

• A transmit MAC module 70a including queuing logic 74 stores data packets in its internal receive FIFO and external memory 36 (A first receiver which stores data packets in a first memory or a second memory; claims 1, 8, 9, and 10). See fig. 3A, Col. 5, lines 20-22, and Col. 6, lines 56-60.

• A expansion port 14 (72b) including queuing logic 74 stores data packets in its internal receive FIFO and external memory 36 (A second receiver which stores a

second data packets in a first memory or a second memory; claims 1, 8, 9 and 10). Also see fig. 3A, Col. 5, lines 20-22, and Col. 6, lines 56-60.

• A transmit MAC module 70c including dequeuing logic 76 transfers data packets from external memory 36 to its internal transmit FIFO (A first output which outputs a first subset of the first data packets and the second data packets; claims 1, 8, 9, and 10). See fig. 3A, and Col. 6, lines 60-63.

• A transmit expansion port 14 (72d) including dequeuing logic 76 transfers data packets from external memory 36 to its internal transmit FIFO (A second output which outputs a second subset of data packets; claims 1, 8, 9, and 10). See fig. 3A, col. 5, lines 20-22, and col. 6, lines 60-63.

• An integrated multiport switch 20b comprises a switch subsystem 42 coupled to the receive and transmit MAC modules 70a, 72b, 70c, and 72d (A switch coupled to the first and the second receiver and coupled to the first and the second output for routing the first subset and the second subset to the respective first or second output; claims 1, 8, 9, and 10). See figures 2 and 3A, col. 5, lines 20-22, and col. 6, lines 30-34.

• Three integrate multiport switches, namely 12a, 12b, and 12c. Each integrated multiport switch has an expansion port 30 that contains an expansion input port and an expansion output port. The expansion input and output ports are daisy chained to enable the multiple multiport switches 12 to be cascaded together (A first expansion data-out circuit of the first switching module is connected to a first expansion data-in circuit of the second switching module, and a first expansion data-out circuit of the second switching module is connected to a first expansion data-in circuit of the first

switching module; claims 8 and 9). See fig. 1, and col. 4, lines 33-37.

• Each switch 12 is coupled to 10/100 physical layer transceivers 16 configured for sending and receiving data packets. Each transceiver 16 connects up to 4 network stations (LAN adapters connects to the LANs; claim 10). The packet switch network 10 comprises three switches 12 (A crossbar switch interconnects all LAN adapters and comprises at least two switching modules; claim 10). See fig. 1, and col. 4, lines 18-25.

5. Claims 2-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,501,734 issued to Yu et al (hereinafter Yu) in view of U. S. Pat. No. 5,689,500 issued to Chiussi et al (hereinafter Chiussi).

Regarding claim 2, Yu does not disclose:

• *The first receiver further comprises a set of 'm' data-in circuits for receiving the first plurality of data packets from a plurality of LAN adapters.*

Each data-in further comprising:

• *A first memory for storing the first subset of the first plurality of data packets, and a second memory for storing the second subset of the first plurality of data packets.*

• *A selector for sending each received frame of the first plurality of data packets either to the first memory or the second memory.*

However, Chiussi discloses a representative implementation of a switching node having 6 input port cards 0 to 5 in an input port unit 110 (see fig. 1), comprising:

• An input port card 0 with an ALM 0 interfaces to 0-31 sub-ports 100. See fig. 1, and col. 2, lines 34-41.

• An ABM 0 receives data packets from the ALM 0, determines the destination of the data packets, and stores them separately in output queues out 1 to 5. Also see fig. 1, and col. 2, lines 34-41.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to develop a switching module having a first receiver with first and second memories, a second receiver with first and second memories, a first output, a second output, a switch that connects the first and the second receivers and first and second outputs together, and the first receiver having a set of "m" data-in circuits that comprise a first memory, a second memory, and a selector, for a key reason. Since a multiport LAN switch may connect to network stations and gateways that have different data rates (such as 10 Mbps, 100 Mbps, or 1Gbps), the first and second memories in the first and second receivers will allow the switch to selectively forward the data packets among the network stations and gateways without having to concern with data loss as taught by Yu. See col. 3, lines 33-43.

Regarding claim 3 Chiussi further discloses the switching node is an ATM switch with an ATM layer manager and an ATM buffer manager integrated circuits (data packets are sized as ATM data). See col. 2, lines 28-31, and lines 45-46.

Regarding claim 4 Chiussi further discloses the switching node, comprising:

• An output port card 0 with an ALM 0 interfaces to 0-31 sub-ports 160 (the first output comprises a set of 'p' data-out circuits for receiving the first subset of the first plurality of data packets and the second plurality of data packets). See fig. 1.

• A routing and arbitration 305 within a switch module ASX (the switch comprises a controller for configuring at each time period a plurality of address lines to route the first subset of the first plurality of data packets and the second plurality of data packets to the appropriate data-out circuit according to the additional byte configuration). See fig. 3, and col. 3, lines 29-32.

Regarding claim 5, Chiussi discloses the switching node, comprises:

• An output port card 1 with and an ABM 1 and an ALM 1 interface to 0-31 sub-ports 160 (the second output comprises a set of 'n' data-out circuits for receiving the second subset of the first plurality of data packets and the second plurality of data packets). See fig. 1, and col. 2, lines 35-41.

• The ABM 1 receives data packets from the switching module ASX, buffers them separately in sub port queues 1 to 31, and then forwards them to the ALM 1 (each expansion data-out circuit comprise storage for storing the second subset of the first data packets received from the corresponding data-in circuit). Also see fig. 1.
Regarding claim 11 (original), in addition to disclose the limitations in claim 10 discussed earlier, Yu further discloses the switch is in a packet switched network, such as an Ethernet (IEEE 802.3) network. However, the switch is also applicable to other types of packet switched systems (at least one of the LANs transmits a plurality of data

frames to another one of the LANs through the crossbar switch, each frame comprising data packets). See col. 3, lines 19-24. Furthermore, Chiussi discloses the switching node is an ATM switch with an ATM layer manager and an ATM buffer manager integrated circuits. See col. 2, lines 28-31, and lines 45-46.

Regarding claim 12, Yu discloses a method for routing data packets having Local Area Networks interconnected by a hub including LAN adapters connected to the LANs and a crossbar switch, comprising:

• A switch 12a couples to 10/100 physical layer transceivers 16 configured for sending and receiving data packets. Each transceiver 16 connects up to 4 network stations (LAN adapters connects to the LANs). The packet switch network 10 comprises three switches 12 (A crossbar switch interconnects all LAN adapters and comprises at least two switching modules). See fig. 1, and col. 4, lines 18-25.

• A transmit MAC module 70a including queuing logic 74 stores data packets in its internal receive FIFO and external memory 36 (A first receiver which stores data packets in a first memory or a second memory of the first receiver). See fig. 3A, col. 5, lines 20-22, and col. 6, lines 56-60.

• An expansion port 14 (72b) including queuing logic 74 stores data packets in its internal receive FIFO and external memory 36 (A second receiver which stores a second data packets in a first memory or a second memory). Also see fig. 3A, col. 5, lines 20-22, and col. 6, lines 56-60.

• A transmit MAC module 70c including dequeuing logic 76 transfers data packets from external memory 36 to its internal transmit FIFO (A first output which outputs a first subset of the first data packets and the second data packets). See fig. 3A, and col. 6, lines 60-63.

• A transmit expansion port 14 (72d) including dequeuing logic 76 transfers data packets from external memory 36 to its internal transmit FIFO (A second output which outputs a second subset of data packets). See fig. 3A, col. 5, lines 20-22, and col. 6, lines 60-63.

• An integrated multiport switch 20b comprises a switch subsystem 42 coupled to the receive and transmit MAC modules 70a, 72b, 70c, and 72d (A switch coupled to the first and the second receiver and coupled to the first and the second output for routing the first subset and the second subset to the respective first or second output). See figures 2 and 3A, col. 5, lines 20-22, and col. 6, lines 30-34.

Chiussi further discloses:

• An ATM cell header 501 contains vpi 502 and vci 503 for routing cell to its destination output port (each data packets have a fixed bytes size with one byte containing the respective final destination address). See fig. 5.

• Input port unit 110 receives data packets (receiving data packets within the first switching module). See fig. 1.

• The switching node assigns a vp base value, between vp base and vp base plus max_vpi, in the LUT 1 table for switching the income cells to the correct destination

output ports (comparing the final destination address a switch module address range of the first switching module). See fig. 8, and col. 7, lines 15-17.

• Stores the cells in memory located in output port card 0 to be sent to the appropriate sub port, or in output port card 1 to be routed to the next switching module (storing data packet into an internal memory of the first switching module for further outputting to the appropriate LAN adapter if the final destination address matches, or storing the data packet in an expansion memory of the first switching module for further routing to the second switching module). See fig. 1.

Regarding claims 6, 7 and 13 Chiussi discloses the switching node assigns a vp-base value, in between vp_base and vp_base plus max _vpi, in the LUT 1 table for switching the income cells to the correct output ports (an address configurator for predefining the address of the switch module as in claim 6; the address of the switch module is a bit configuration to be compared to the module bit configuration of each incoming data packet as in claim 7; assigning a switch module address range as in claim 13). See fig. 8, and col. 7, lines 15-17.

Response to Arguments

6. Applicant's arguments filed on 11/12/2004 have been fully considered but they are not persuasive. The Applicant argued that a first or second memory is integral to the first receiver and cited para. 30 of the Specification. Examiner noted that in claims 1, 8, 9 and 10, the limitation reads "...memory of the first receiver..."). In the broadest

interpretation of the claims, this memory can be interpreted as *coupled* to since in*tegrated* is not explicitly claimed herein. This limitation, in its broadest term, is met by the Yu '734 as discussed in the rejection of claim 1. The Applicant relied upon the same argument in respect to the remainder of the claims.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afsar M. Qureshi whose telephone number is (571) 272 3178.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272 3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AFSAR QURESHI
PRIMARY EXAMINER
April 29, 2005